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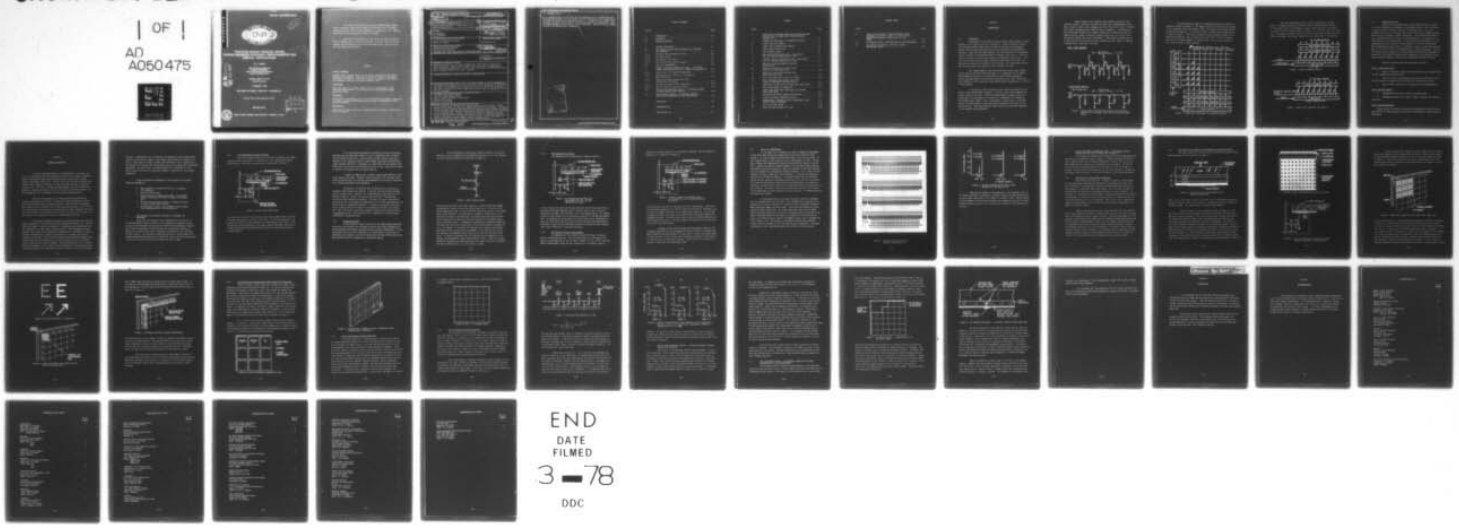

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THIN-FILM BUCKET BRIGADE DEVICE CHARGE-TRANSFER EFFICIENCY IMPROVEMENTS FOR DISPLAY APPLICATIONS

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19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

solid-state flat-panel displays
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cascode active matrix
peripheral addressing

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

Aerojet's approach to improving the charge-transfer efficiency (CTE) of bucket-brigade devices (BBD) for flat panel display applications is described. The task entailed studying candidate BBD configurations, making tradeoff analyses, determining factors which affect BBD CTE efficiency and analyzing display-to-cell interface circuit considerations. Recovery from initial setback in optimizing interface circuitry between BBD and classic active matrix forced an innovative approach involving a new class of active matrix (cascode circuit) to avoid requirement for high-voltage BBDs with their attendant loss of transconductance.

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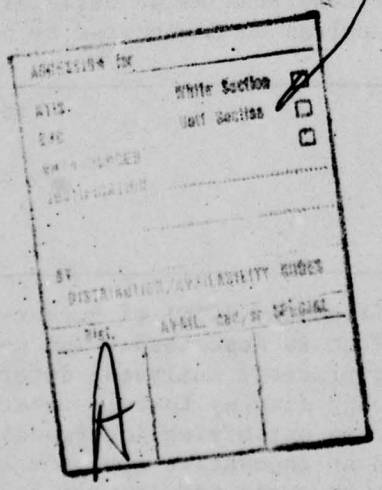
20. ABSTRACT (Cont.)

It is concluded that full TV format display addressing can be achieved with the 99.7% BB CTE attained. This is possible with the new matrix control architecture developed for achieving the required high yield. A program for the design, construction, assembly, and testing of flat-panel displays is recommended as a means of demonstrating the matrix control concept developed. Efforts to further improve the CTE of the BBD are also recommended.



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FIGURES

FIGURES (CONT.)

Section 1

INTRODUCTION

1.1 BACKGROUND

Development of flat panel XY matrix display media capable of alphanumerics, vector graphics and even realtime TV, is being pursued at Aerojet ElectroSystems Company (AESC) Thin Film Devices Laboratory and elsewhere. Several light-emitting and light-modulating technologies are competing for dominance. Some have sufficient inherent cell non-linearities to accommodate direct (cross-bar) XY addressing without crosstalk; others do not. Some have inherent storage to minimize peak luminance requirements; some do not. In all cases active matrices consisting of thin-film transistors within each cell structure are capable of providing these functions. The functionally addressable XY matrix flat panel display is thus technically at hand.

The accomplishments cited above bring into focus a major hurdle in the route to practical display systems, i.e., elimination of the 1000 to 2000 peripheral interconnects necessitated by off-substrate addressing. Studies and experimental investigations instituted in the final task of Contract N00014-75-C-1137 indicated a potentially feasible approach to the solution of this problem.

It is apparent that the display control data stream must be serialized to the maximum extent possible. A one-wire entry would exemplify the process taken to the limit. Practical accomplishment, however, will be attained when the interconnects are reduced to a manageable, cost effective, and reliable small number. Such a distribution circuitry must be efficient and its technology must be compatible with the extended area nature of the display per se. Thin-film-transistor (TFT) circuitry lends itself admirably to the extended area requirement.

Classic digital shift register (DSR) schemes suitable for the requisite serial to parallel conversion function can be implemented in thin film. However, these classic schemes tend toward high device counts, attendant real estate consumption, and prohibitive power consumption. Fortunately, the thin film bucket brigade device (BBD) configuration, developed at AESC, is a highly efficient serial-to-parallel converter which has a low device count and imposes minimal real estate requirements. DSRs contain a minimum of six to well over 24 active devices per bit; the BBD only two. Figure 1 compares a minimum device count DSR to the BBD.

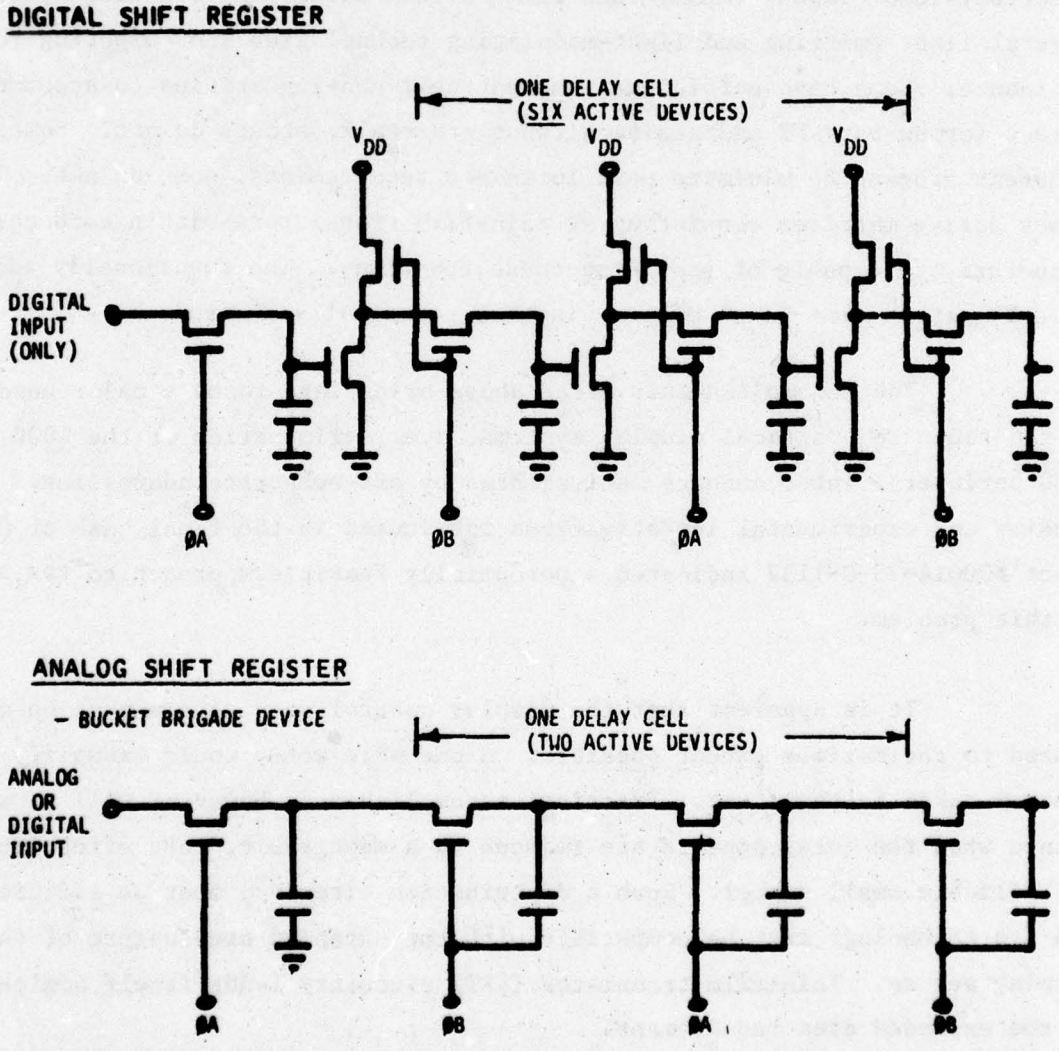

FIGURE 1 DEVICE COUNT OF MINIMUM COUNT DIGITAL SHIFT REGISTER COMPARED WITH THE ANALOG SHIFT REGISTER BUCKET BRIGADE DEVICE

The generalized "peripheral" XY addressing problem is usually illustrated as shown in Figure 2. The sampler shown at the bottom of the figure can be configured using either BBDs or DSRs. The classic (scan mode) form is illustrated in Figure 3. In contrast to this, a direct video transport mode is shown in Figure 4. This mode of operation can be attained by means of an analog shift register, such as a BBD, but not by a DSR. It will be noted that only one storage register is required since, in this case, the BBD itself forms the first storage register.

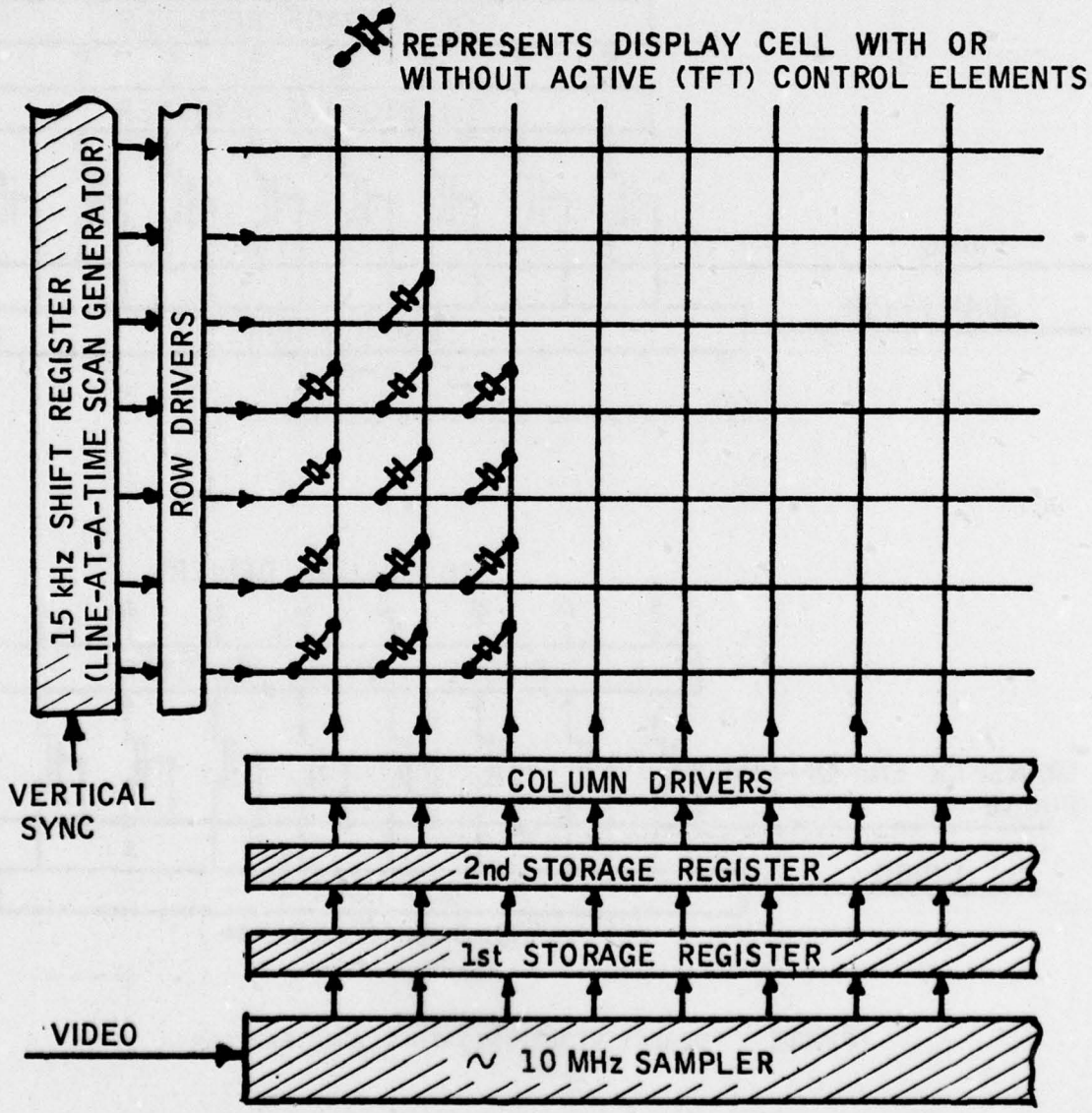

FIGURE 2 GENERALIZED "PERIPHERAL" XY ADDRESSING PROBLEM

The power dissipation and real estate advantages of the BBD make it a leading contender in XY matrix control implementations; however, in its present state of development it cannot service the 500 or so columns or rows of a full TV format because of finite loss of fidelity with each transfer. The measure of signal fidelity is given by the charge transfer efficiency (CTE) of the BBD. This subject brings us to the objectives of this program.

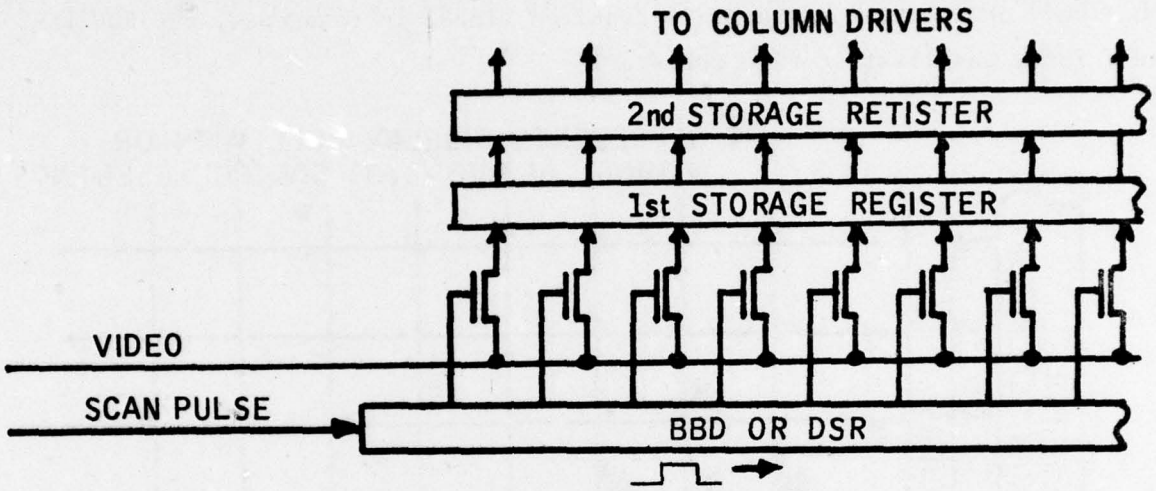

FIGURE 3 CLASSIC SCAN MODE SAMPLER

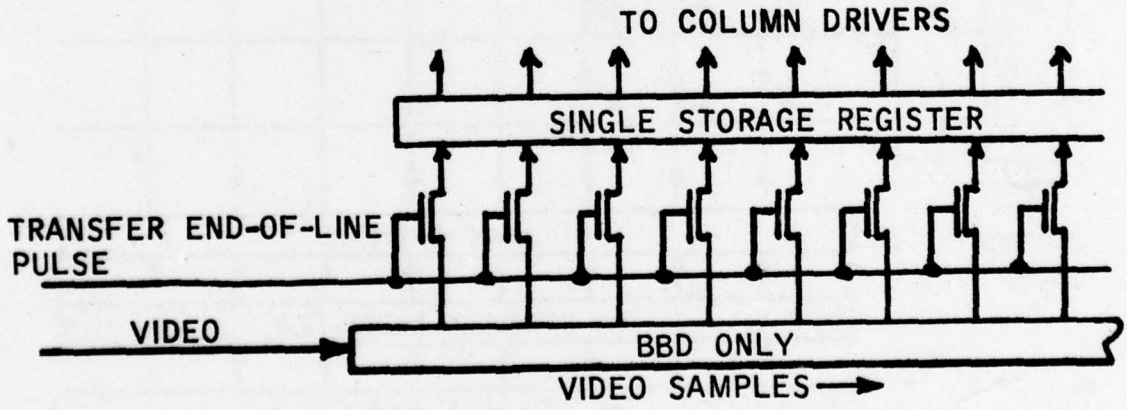

FIGURE 4 DIRECT VIDEO TRANSPORT MODE SAMPLER

1.2 PROGRAM OBJECTIVES

Going into this program AESC's stated objectives were, in part, ..."a truly significant advancement of the present state of the art relative to charge transfer efficiency (CTE) of the BBD must ensue... The AESC laboratory has thus far achieved a CTE of 99 percent at room temperature and 99.9 percent at cryogenic (-100°C) temperature. The minimum useful CTE for the ...application is 99.9 percent at room temperature. The design goal is 99.98 percent at room temperature. It is estimated that attainment of a CTE compatible with full real-time TV requirements is a two-year undertaking. This seven-month technical effort is intended to result in sufficient advancement in the state of the art to demonstrate the ultimate potential... The overall purpose of the program is to further develop the thin film technology required for a flat panel TV display and to demonstrate the feasibility of producing complete displays of this type by integrated thin-film processes."

Specific technical tasks were specified as follows:

Task 1--Technology Studies

A. Study to determine candidate BBD configurations and tradeoff analysis for implementation consideration.

B. Study of factors affecting BBD charge transfer efficiency, implications relative to mechanization and analysis of experimental results.

C. Study of BBD to display cell interface circuit considerations.

Task 2--BBD Development

A. Implementation and test of Task 1.A candidate BBDs.

B. Implementation and test of Task 1.C BBD to display cell interface circuitry.

Task 3--BBD Demonstration

Design, build, and operate in laboratory demonstrations, thin film display devices for demonstrating the function and performance of BBD peripheral addressing.

Section 2

PROGRAM ACHIEVEMENTS

In terms of maximum benefit to the advancement of XY matrix control, it is fortunate that this program was structured to include the implications of real-world display matrix characteristics, rather than a charge transfer improvement effort only. Had the latter been the case, we might have ended up with a higher efficiency, but would not have been able to take advantage of it. The effort to devise optimum interface circuitry between the BBD and a classic active matrix forced a fresh view of the overall matrix control problem and its relationship to overall system considerations.

Prior to this program, active matrices had been addressed and driven by off-substrate circuitry. Voltage and power requirements to perform these functions were thus of secondary concern. However, these requirements were found to be the "pacing" factor during the present program. As it turned out, the voltage problem had such a severe impact on charge transfer efficiency, that a major part of the program effort had to be devoted to the creation of a new class of active matrix as a means of eliminating the problem.

All system configuration studies on this program have been directed toward achievement of full normal and high resolution TV formats, i.e., 500 and 1000 line formats. Insofar as possible, no configuration was pursued that was not appropriate to a wide range of physical sizes. This philosophy has been adhered to as a means of preventing the consideration of techniques of limited ultimate usefulness and to hasten the recognition of problems that partial solutions tend to hide. Thin film EL has been the primary display medium under consideration and the desirability of an active matrix as part of any matrix control scheme has been tacitly assumed. These guidelines have led to some far reaching conclusions. One of these is the improbability of anyone ever economically producing full TV format matrix control circuitry with a full TV format

mask set. Consideration of the difficulty of designing row and column drivers capable of driving full format row and column capacitances and a desire to be able to "distribute" the BBDs to reduce CTE requirements led to recognition of the absurdity of thinking that matrix addressing was synonomous with "peripheral" addressing. The mask, driver, and BBD problems led to synthesis of a new matrix control architecture potentially capable of resolving all the problems enumerated.

Study and hardware achievements of this program are discussed under the headings of:

a. The "Cascode" Active Matrix Solution to a Dominant CTE Impediment

b. Basic CTE Improvements

c. Display Electronic Segmentation (DES): A New Matrix Control Architecture for Full TV Format With Present CTE

d. The DES Step-and-Repeat Display: A Possible Approach to Matrix Control Mask Viability

e. The DES Mosaic Display: An Extremely Versatile High-Yield Implementation of DES Architecture.

2.1 THE "CASCODE" ACTIVE MATRIX SOLUTION TO A DOMINANT CTE IMPEDIMENT

Going into this program it was recognized that new factors affecting BBD charge transfer efficiency would probably be unearthed, but not one that could invalidate the whole idea of BBD display addressing. However, such a factor encountered in the first month of the program resulted in a search for a solution that was not completely resolved until the last month of this contract. Its resolution reinstated the BBD as a viable display addressing implementation and moreover resulted in a new, versatile active matrix ...one that can be controlled by low voltage TFT, TTL, or MOS.

2.1.1 The High-Voltage Transport Problem

One of the program tasks was to interface the BBDs to the display elements via an active matrix. We will refer to the standard and typical active matrix as the classic active matrix, illustrated in Figure 5.

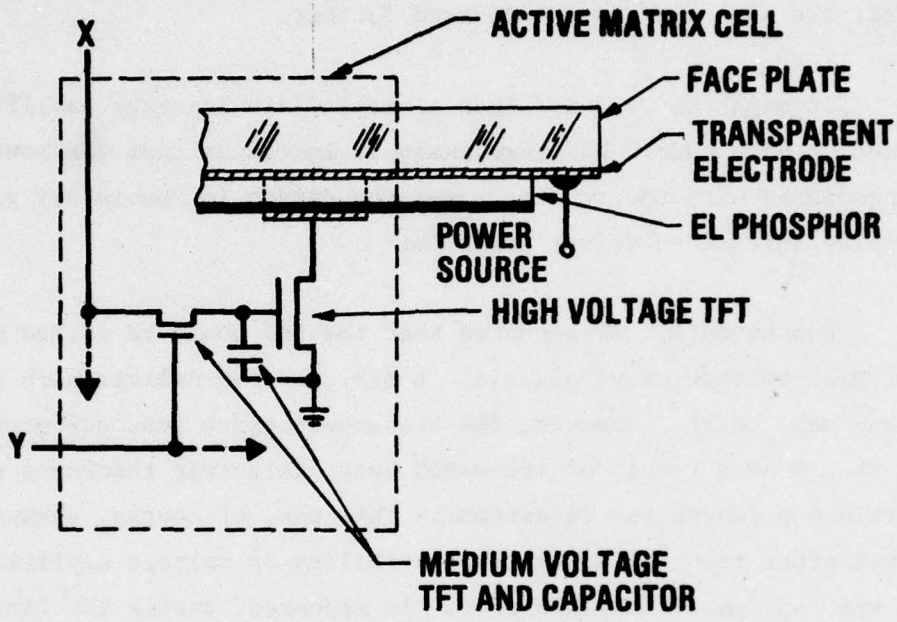

FIGURE 5 CLASSIC ACTIVE MATRIX CELL

For thin film EL, powder EL and certain other major display media, the X and Y address levels are of the order of 50 volts. It was known going into the program that from CV^2f power dissipation considerations of the BBDs, a voltage step-up would be required at the output nodes of the BBDs. What was not properly appreciated was the difficulty involved in providing the step-up or amplification.

It is theoretically possible to provide the step-up function by assuring that the final BBD transfer is into a capacitance that is smaller, by the desired step-up ratio, than the main line BBD transfer capacitors. Analysis of this approach results in BBD designs containing unrealistically large transfer capacitors, requirement for larger TFTs and thus greater real estate and loss of yield and reliability or loss in CTE. Since none of these is desired, the approach was not pursued further.

It might be reasoned that a simple, single-stage amplifier could be provided at each node. However, analysis indicates that the power dissipation associated with the requisite gain-bandwidth is absolutely prohibitive for a display-integrated driver amplifier.

Subsequently, it appeared that the BBD would be called upon to transport high-voltage drive signals. A BBD that can deliver such voltages can be, and was, built. However, the transconductance loss suffered in the transfer stages as a result of increased gate dielectric thickness and source-drain gap length was disastrous. This was, of course, analytically anticipated after recognizing the impractibility of voltage amplifiers, but the solution was not immediately apparent. It appeared, during the first month of the program, that we had taken a step backward in our effort to enhance CTE. Basic CTE (from a low-voltage academic viewpoint) had suddenly become a non-pacing problem. The problem was how to ameliorate the high-voltage contribution to diminished CTE.

2.1.2 The Basic Cascode

It was decided to take a hard look at the high-voltage switching TFT of the active matrix cell of Figure 5, with an eye toward increasing its transconductance and thereby reducing the drive voltage requirements. It was ascertained that brute force widening of the semiconductor channel was not compatible with realistic real estate allocations and that off-resistance and gain-bandwidth would be degraded to a prohibitive degree.

The gain-bandwidth consideration brought to mind a very old but effective circuit configuration for enhancing this factor, i.e., the cascode. The basic cascode structure is illustrated in Figure 6.

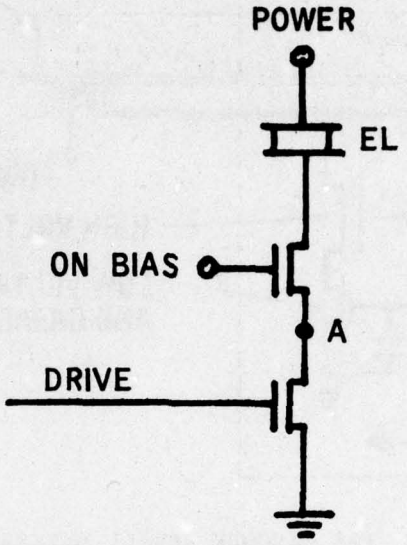

FIGURE 6 BASIC CASCODE CIRCUIT

The structure has some interesting properties. Without going into lengthy derivations, it is more or less intuitively evident that if the top TFT is biased sufficiently "ON", the lower TFT will then be in control of the ON-OFF state of the structure. At first glance it might be thought that if the lower TFT is driven to the OFF state, all voltage would be across this TFT. Closer scrutiny will reveal that the lower TFT acts as an off-bias source load to the upper device. Consequently, assuming zero threshold voltage for the upper TFT, point "A" can only rise to the on-bias level of the upper device. For example, if the upper TFT represents the original active matrix switching TFT with a normal drive requirement of 30 volts and has 30-volt bias applied, the maximum potential seen by the lower TFT will then be 30 volts. It should be apparent that the lower TFT can be designed as a low-voltage, and, consequently, high-transconductance device. That is, the gate dielectric thickness and source-drain gap can be small relative to the upper TFT and the drive level can be significantly reduced.

2.1.3 The Cascode Active Matrix

The foregoing can be illustrated as shown in Figure 7.

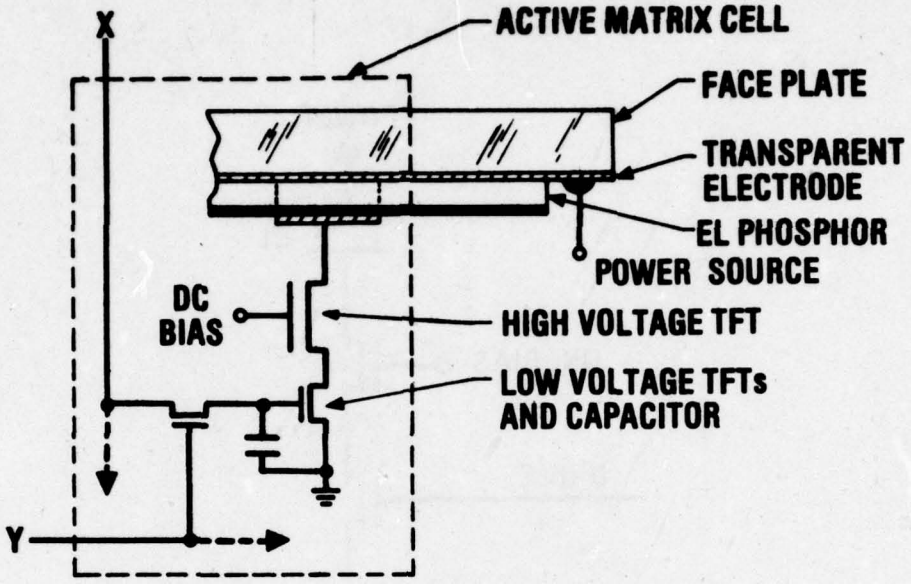

FIGURE 7 THE CASCODE ACTIVE MATRIX CELL... LOW VOLTAGE TFT, TTL, AND MOS COMPATIBLE AT X AND Y

It will be noted that both the storage capacitor and the logic gate TFT are now very low-voltage components and, of course, since X and Y levels are supplied by the BBDs, then the BBD is also a low-voltage device. The ramifications of the structure go far beyond the resolution of the BBD CTE impediment. By reducing the active matrix cell drive level we have materially reduced the CV^2f power required from the drivers and thus have significantly diminished a major display addressing dissipation problem that has received very little recognition in existing literature.

2.1.4 The "Virtual" Cascode Active Matrix

An examination of the cascode structure of Figure 7 brings to mind an interesting question. That is, what function is performed by the metallic interconnection of the two TFTs? Couldn't it just as well have been made of infinitesmal length and then "thrown out"? In reality, since it

performs no required function, it can indeed be removed. The resulting configuration is illustrated in Figure 8.

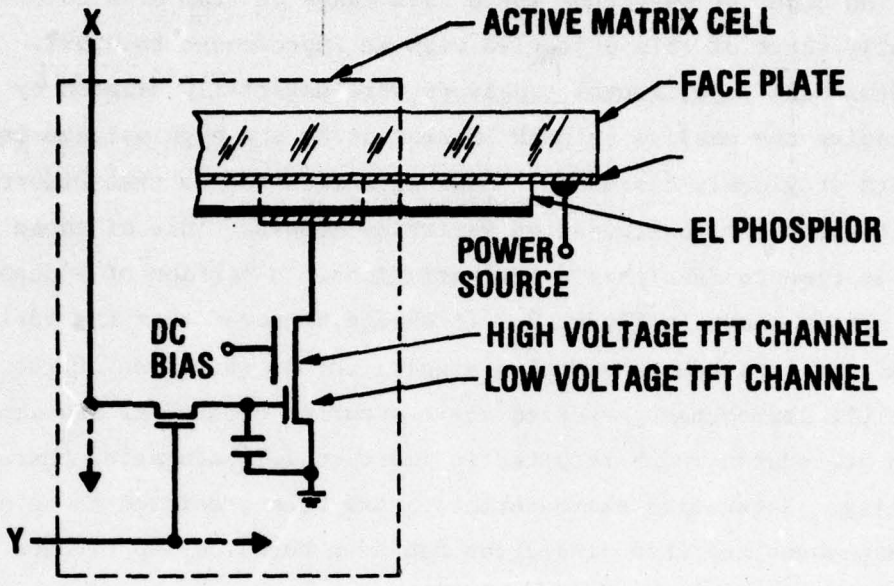

FIGURE 8 "VIRTUAL CASCODE" ACTIVE MATRIX CELL... LOW VOLTAGE TFT, TTL, AND MOS COMPATIBLE AT X AND Y

The obvious gain has been in reducing real estate requirements. This could not have been possible with a "normal" (equal gate dielectric thickness) cascode for the simple reason that the two gates would short out. In the case of Figure 8, however, the gates can be deliberately overlapped slightly for alignment purposes. The cascode and virtual cascode structures discussed are not analytical projections. On this program, they have been fully developed into actual thin film hardware.

Although we have walked through that development rapidly in the foregoing discussion, actual development of viable active matrix geometries, mask design, and testing, followed by reiterations to achieve the desired high-voltage stand-off and low-voltage drive performance, consumed a large span of the time available on this short program. Regrettably this did dilute the pursuit of some basic CTE enhancement ideas.

2.2 BASIC CTE IMPROVEMENTS

It was hoped that a minimum of an order of magnitude improvement in CTE would ensue during the program despite the short technical effort schedule. An order of magnitude would have taken us from 0.99 to 0.999. We fell slightly short of this objective with an improvement to 0.997. Certain basic academic and experimental endeavors were materially diluted by the effort to resolve the massive setback brought on by the high-voltage transport requirements previously discussed. Mask sets required in that effort delayed the sets intended for configuration variation studies. One of these sets was completed in time to fabricate a few variations. A portion of a deposition from this set is shown in Figure 9. It should be noted that the variation studies had not resulted in anything significant by the close of the program. The modest CTE improvement reported above occurred because of new improved deposition procedures which resulted in improved TFT saturation characteristics and stability. Saturation characteristics had been predicted to be a factor in CTE enhancement and this prediction has been borne out to perhaps the degree one might have surmised.

As previously noted, the stated objectives included a statement that the minimum useful CTE was 0.999. This statement was predicated on the notion that it would be desirable to service all 512 columns/rows by means of BBDs having that number of service nodes. The notion was graphically illustrated, as shown in Figure 10. The output amplitudes shown for the 508th, 510th, and 512th nodal points (N) are for a singular scan pulse injection and depict conditions extant at the nodes at the moment the scan pulse has arrived at the 512th position, where it presumably would be used to address the 512th column or row. The outputs at the 508th and 510th nodes represent residue from the transport of the scan pulse, and are undesirable. The marginal aspect of a 512 stage BBD having a CTE of 0.999 is clearly evident.

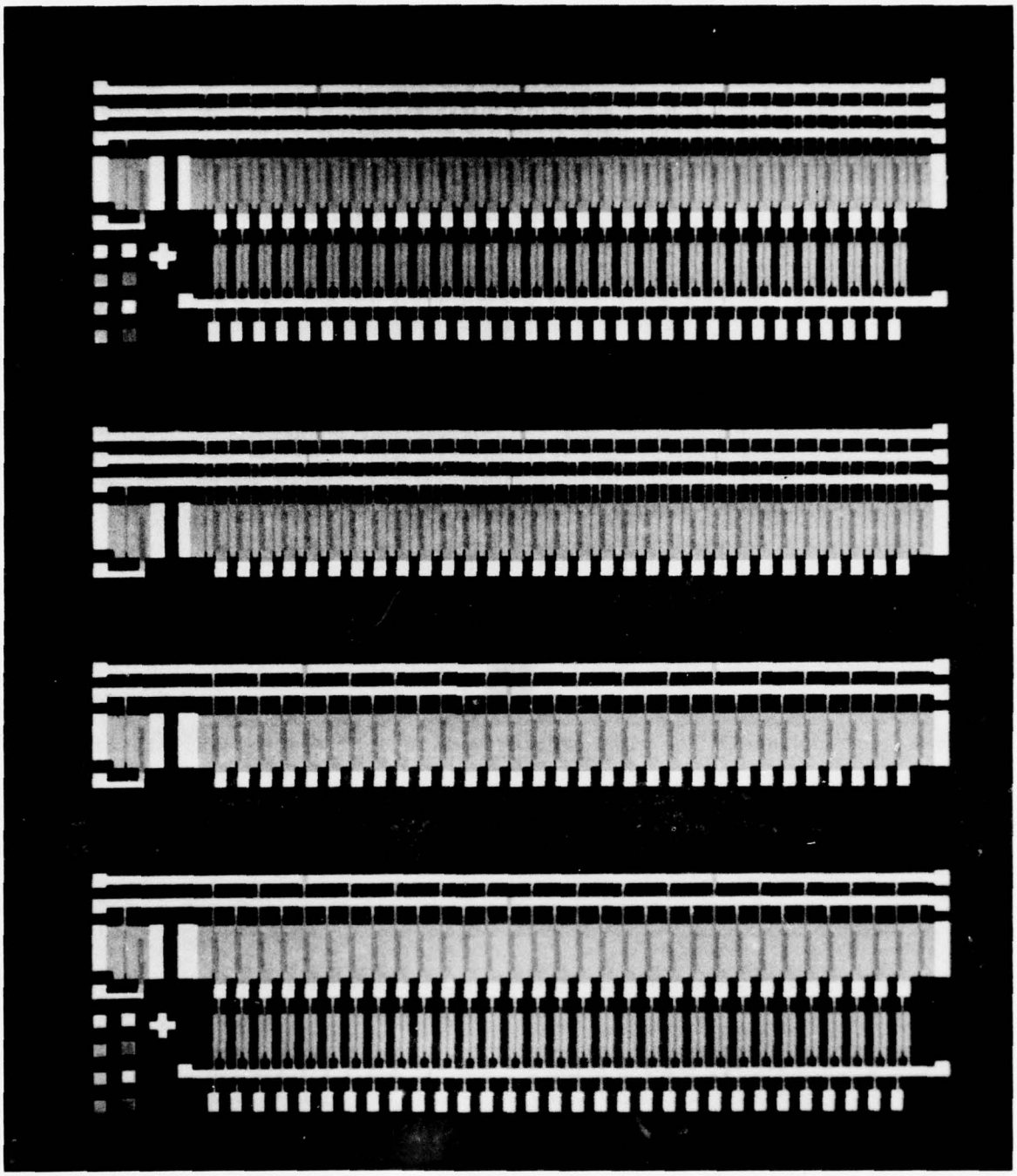

FIGURE 9 PORTION OF BBD CONFIGURATION VARIATION DEPOSITION SET

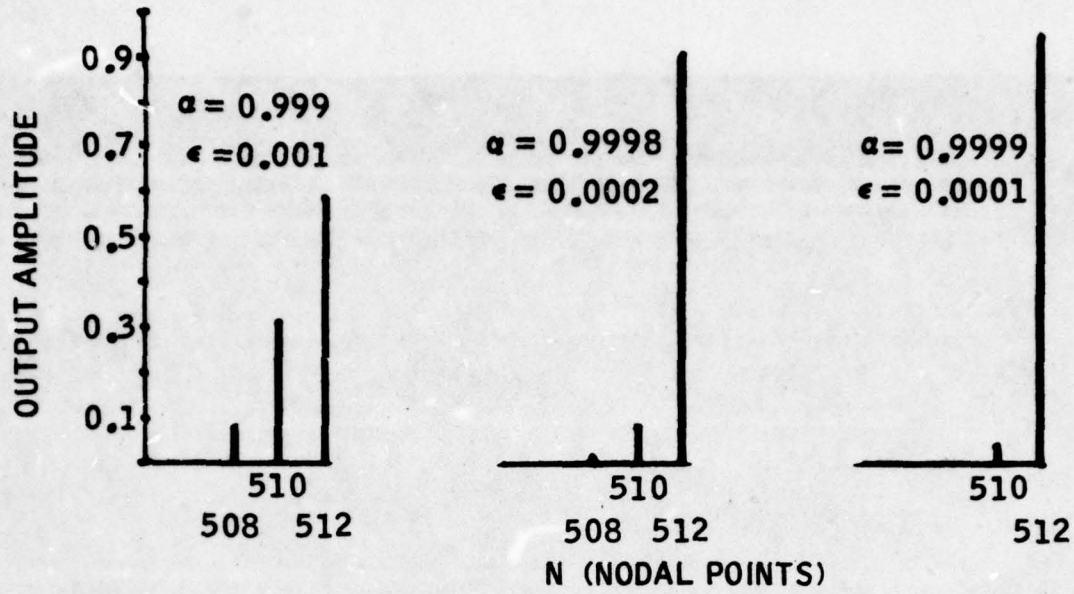

FIGURE 10 SPATIAL DISTRIBUTION FOR SINGLE PULSE ARRIVING AT 512TH NODE VS CTE

What was not evident at the beginning of this program is that it is neither necessary nor desirable to address displays via BBDs having column (or row) stage counts equal to the number of columns or rows. The net result of this finding is that present CTE values are compatible with full TV format. Program studies leading to this conviction are outlined in the following subsection.

2.3 DISPLAY ELECTRONIC SEGMENTATION (DES): A NEW MATRIX CONTROL ARCHITECTURE FOR FULL TV FORMAT WITH PRESENT CTE

It has long been assumed that XY matrix control was synonomous with the notion of "peripheral" control circuitry. Display-integrated peripheral control implies that both the signal distribution circuitry and a driver for each column and row resides at the "periphery" of the display. This notion has led to ever increasing difficulty as the number of rows and columns increases. At the time of this writing no one has ever succeeded in integrating the matrix control circuitry, for a full TV format, on the display periphery.

2.3.1 Limitations of "Peripheral" Addressing

The difficulty accrues from a number of factors. As the number of rows and columns increases, the difficulty of providing low loss X and Y lines increases. The capacitance seen by the drivers increases, along with the frequency of addressing these capacitances. The CV^2f power that must be dissipated by the drivers thus increases due both to C and f increases. In addition, as f increases the time allowed to address decreases and this implies a requirement for decreased driver internal resistance to combat the rise and fall times associated with the RC products. And, in the case of a BBD-driven display, the requirements for increased CTE rise in direct proportion to the number of rows and columns.

Study on this program has led to the conclusion that the accepted brute force peripheral approach is counter productive and that there are better ways to accomplish the matrix control function. The basic philosophy of a new approach is discussed in this subsection and subsequent subsections develop the idea of physical implementation. Since it is the display "system" that must be reexamined, and not just the matrix control function in-vacuo, we need a display-medium vehicle to aid in the discussion. We choose to start with our own thin film EL, firstly because it is the medium that has been used on this program; secondly, because it has historically been difficult to drive; and thirdly, it is rapidly becoming the leading flat-panel display medium.

2.3.2 Thin Film EL As a Vehicle for Discussion of New Possibilities

The basic structure of our thin film EL containing an ambient-light absorbing black layer is depicted in Figure 11.

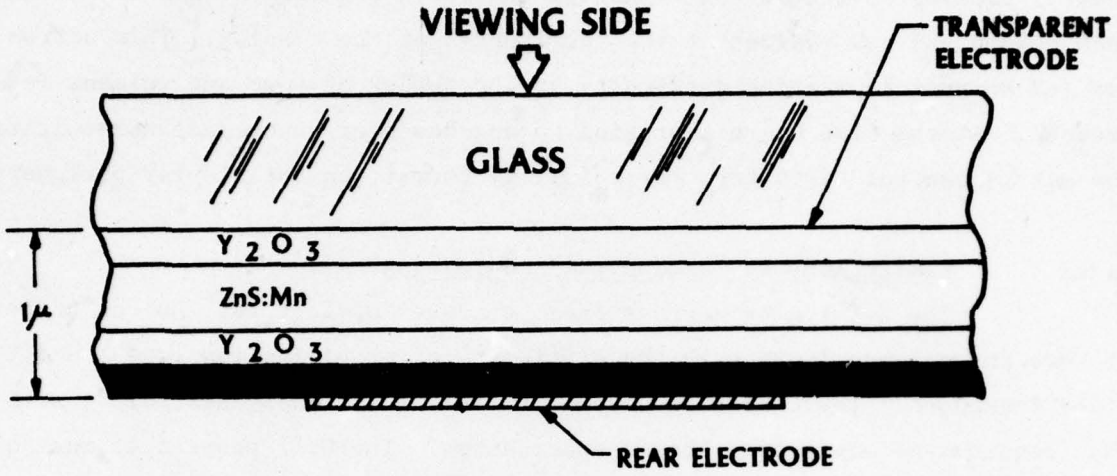

FIGURE 11 BASIC THIN FILM EL WITH AMBIENT-LIGHT ABSORBING BLACK LAYER

This is an ac EL structure since the emitting layer is sandwiched between two dielectric layers. The entire structure is vacuum deposited on to the glass substrate shown. The figure depicts a single display element.

A basic XY matrix of such elements is shown in Figure 12. The plan view of the back (non-viewing) side shows the isolated rear electrodes. The front, with all elements "OFF", would simply appear totally black, since the black layer prevents ambient light from being reflected from the rear electrodes, otherwise the structure is totally transparent. The extent of the rear electrodes determines the extent of the radiating element. The elements can be tightly spaced or generously separated, as illustrated in Figure 12. When spaced as in the figure, it is possible to deposit an active matrix, such as that of Figure 5, so that the matrix occupies the space between the rear electrodes. An active matrix such as shown in Figure 13 may be used to eliminate the requirement for access to the transparent electrode shown in Figure 12.

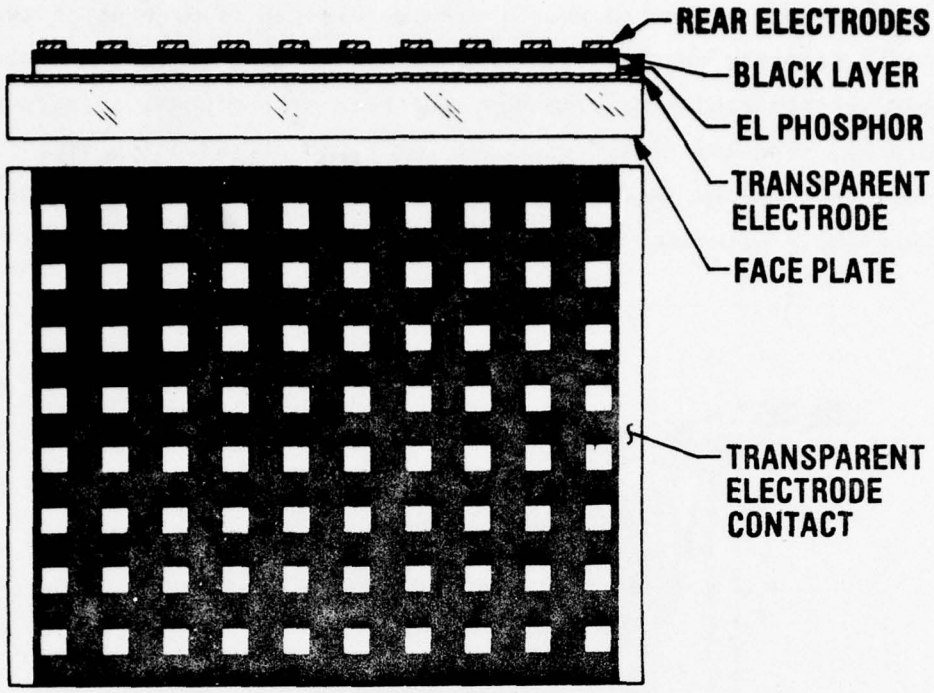

FIGURE 12 BASIC BLACK LAYER THIN FILM EL XY MATRIX

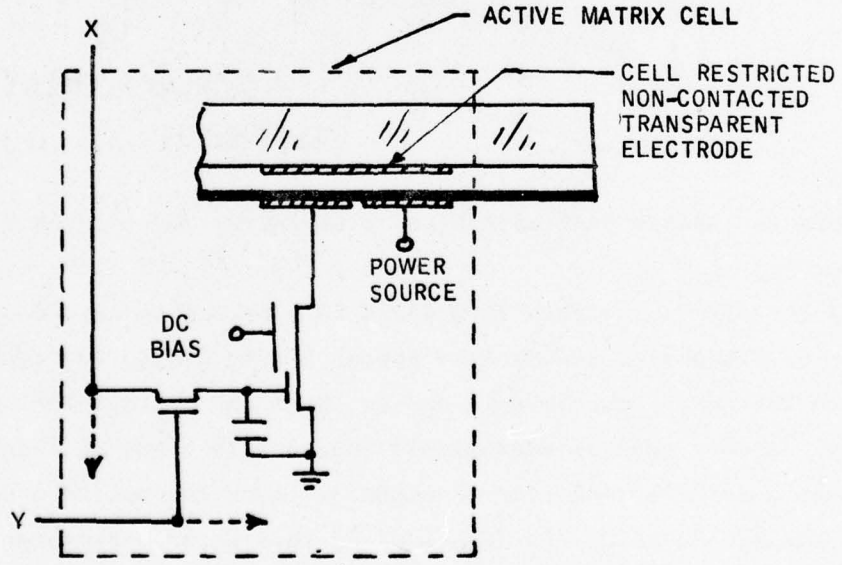

FIGURE 13 SPLIT ELECTRODE ACTIVE MATRIX CELL WHICH OBVIATES TRANSPARENT ELECTRODE ACCESS

It will be noted that a viewing element is made up of two closely spaced half elements that are electrically in series. When the active matrix is placed between radiating elements, the rear of the panel appears as shown in Figure 14. The low fill factor, or low ratio of radiating area to non-radiating area reduces legibility in some applications; in others it is simply not esthetically pleasing.

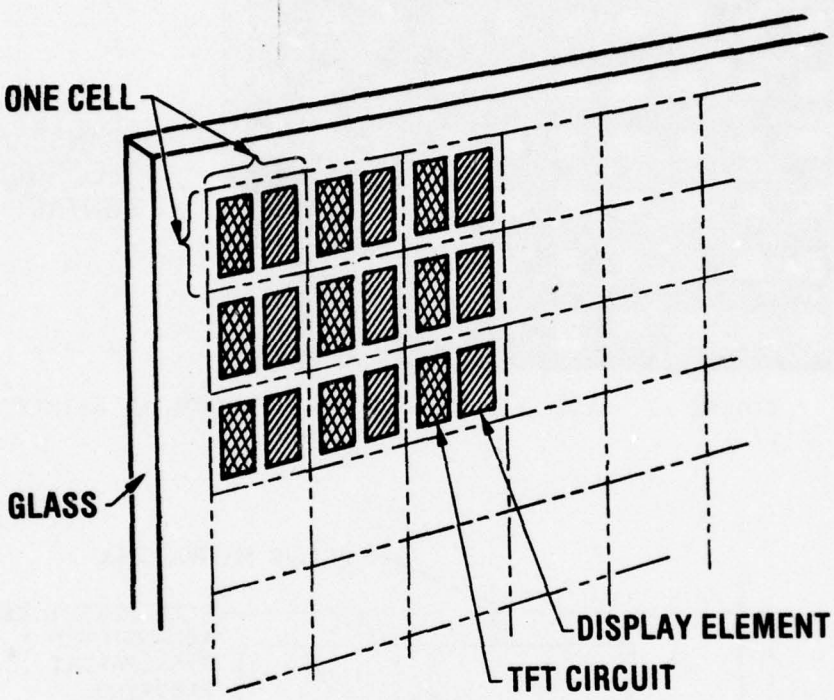

FIGURE 14 SHARED REAL ESTATE LOW FILL FACTOR PANEL (REAR VIEW)

The fill factor effect on legibility would be expected to appear as illustrated in Figure 15. The shared real estate approach also limits the real estate available to the active matrix cell and to the X and Y lines that must traverse the display. A more generally desirable approach is shown in Figure 16. In this approach a thick low-dielectric-constant layer is applied over the display per se and the active matrix is deposited on this layer making contact with the rear electrodes through the layer. Materials and processes suitable for this dielectric layer were evolved during this program. In this coaxial approach, sufficient real estate is generally available to include bucket brigade

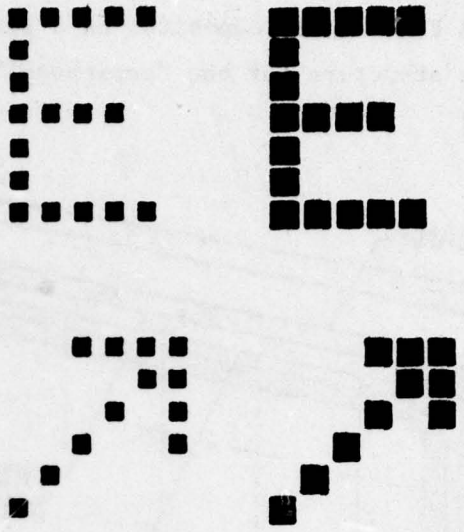

FIGURE 15 FILL FACTOR EFFECT ON VIEWABILITY

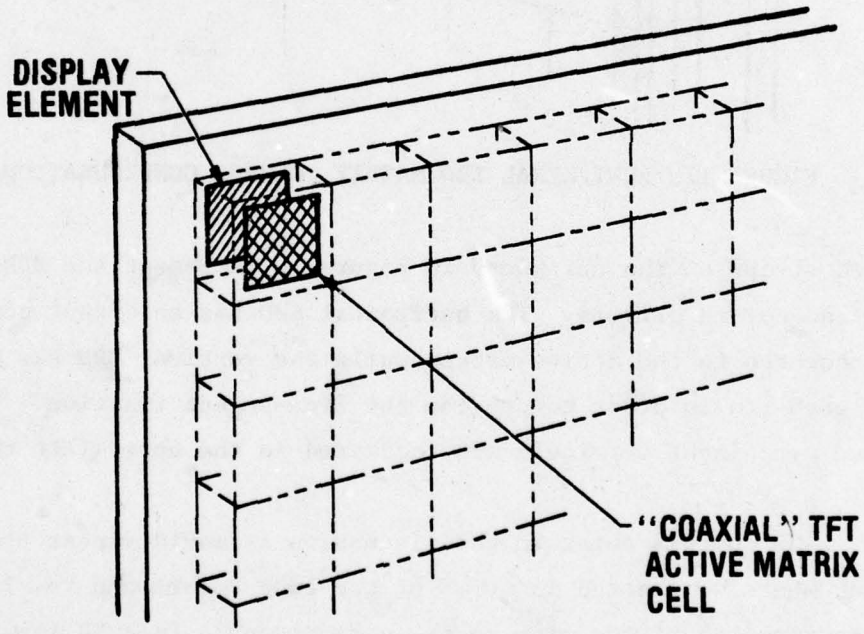

FIGURE 16 COAXIAL NON-SHARED REAL ESTATE HIGH FILL FACTOR PANEL (REAR VIEW)

device (BBD) signal distribution stages within the active matrix cells. In any event, the required BBDs can be deposited on a second dielectric layer if more appropriate. The structure for the "peripheral" matrix control case is depicted in Figure 17.

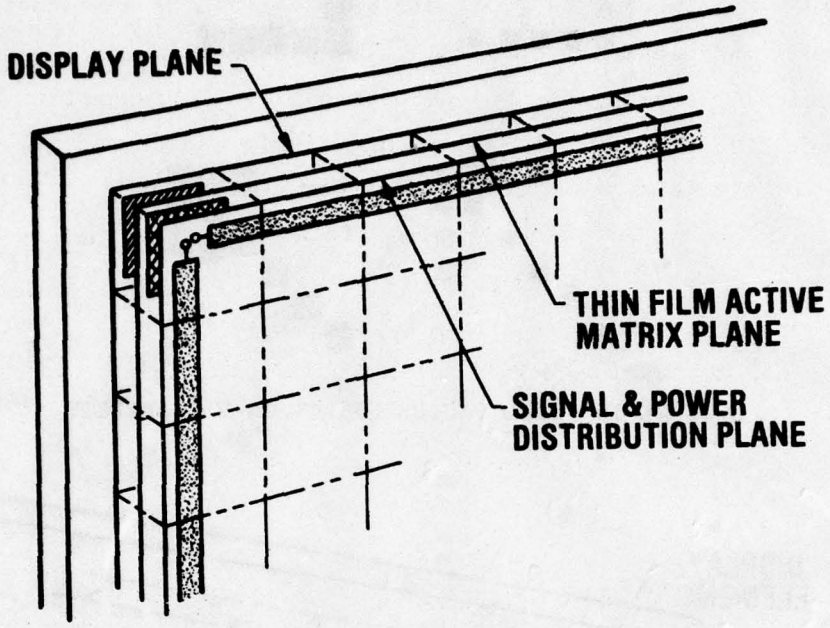

FIGURE 17 PERIPHERAL BBD MATRIX CONTROL CONFIGURATION

The shaded strips on the periphery in Figure 17 represent the BBDs and associated row and column drivers. The horizontal BBD has an output node at each column connected to the active matrix while the vertical BBD has an output node for each row in order to provide the line-select function. The serial signal and sync input terminals are indicated in the upper left corner.

Up to this point in the discussion it would appear that we are right back where we started in terms of the long column and row lines and long BBD chains required if the picture is to represent a full TV format display. It is at this point that we take a fresh new view of what Figure 17 might represent.

2.3.3 Display Electronic Segmentation (DES) Architecture Philosophy

Instead of using a single column and row BBD, the display can be segregated electronically as shown in Figure 18. The dotted lines mark the boundaries of segments at which the X and Y lines (power and signal) are interrupted. Each sector is treated electrically as a self contained display and all sector displays are driven in time-parallel in terms of the signal. The connections required to each sector are minimal, consisting of one signal, one line-select sync, BBD clock lines, and display power and ground. It is important to note that these connections can be available on the back of each sector. In addition, the size of the pads for these connections can be quite large, even terminating in a physical connector, if desired. It is, of course, obvious that all common power, ground, phase lines, etc., can be provided by means of low-resistance printed circuits such as depicted in Figure 19.

For n sectors, there will be n signal lines in the interconnect harness. If, however, a single serial signal input to the overall display is required, it is possible to provide a silicon (high-speed) 1:n serial to parallel converter on the back of the display for distributing the signal to the n sectors. A silicon BBD could provide this function.

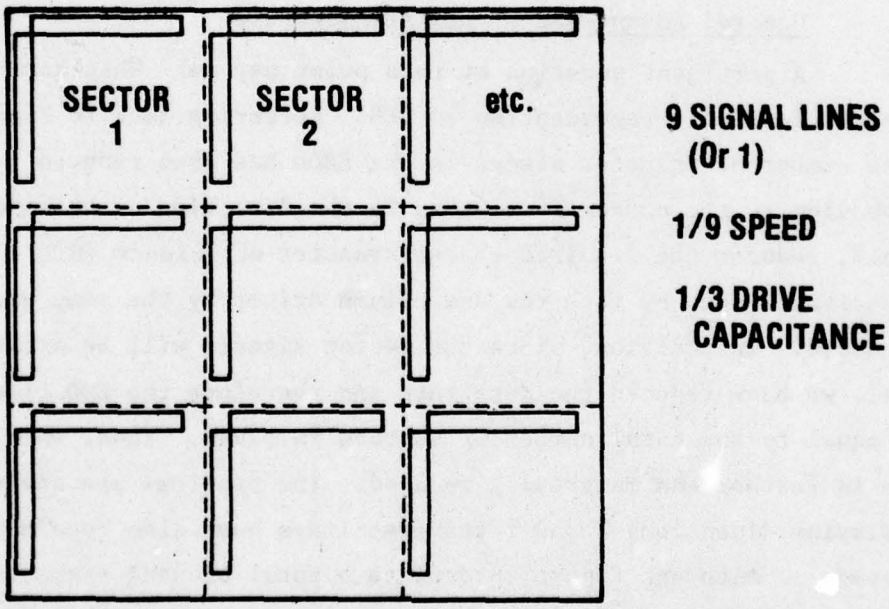

FIGURE 18 DISPLAY ELECTRONIC SEGMENTATION (DES)

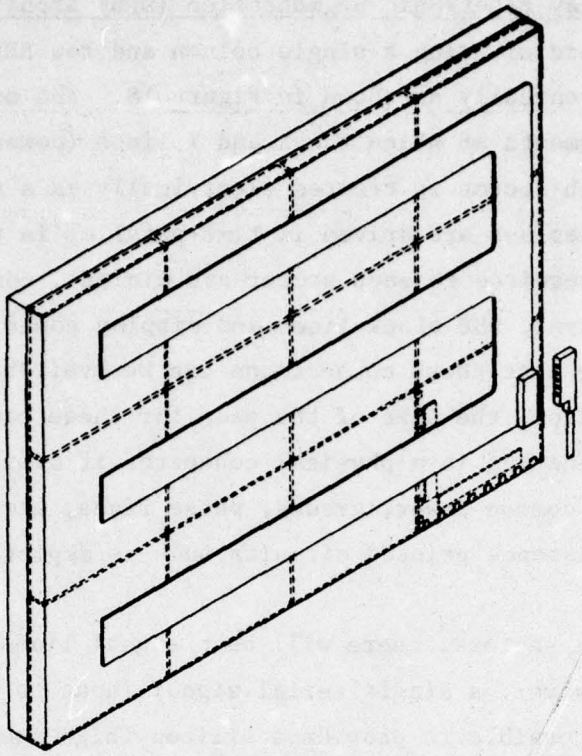

FIGURE 19 ELECTRONICALLY SEGMENTED DISPLAY INTERCONNECT USING PRINTED CIRCUIT TECHNIQUES

2.3.4 General Advantages of DES Architecture

A pertinent question at this point may be: What has been gained by display electronic segmentation or DES? Referring back to Figure 18, note that the number of transfer stages in the BBDs has been reduced by a factor corresponding to the number of sectors in the direction of transport. This, in itself, reduces the required charge-transfer efficiency (CTE) of the devices. The capacitance seen by each row and column driver by the same amount has also been reduced. In addition, since the sector signals will be arriving in time-parallel, we have reduced the data rate and therefore the BBD clock rate by a factor equal to the total number of sectors involved. Thus, the BBD CTE problem is further and materially reduced. The problems associated with very long (display dimension) X and Y traverse lines have also been materially alleviated. Although Figure 18 depicts a total of nine segments, this number is for illustrative purposes only. In principle, the number is selected

to optimize overall system considerations (e.g., Figure 20 illustrates a 36-segment format).

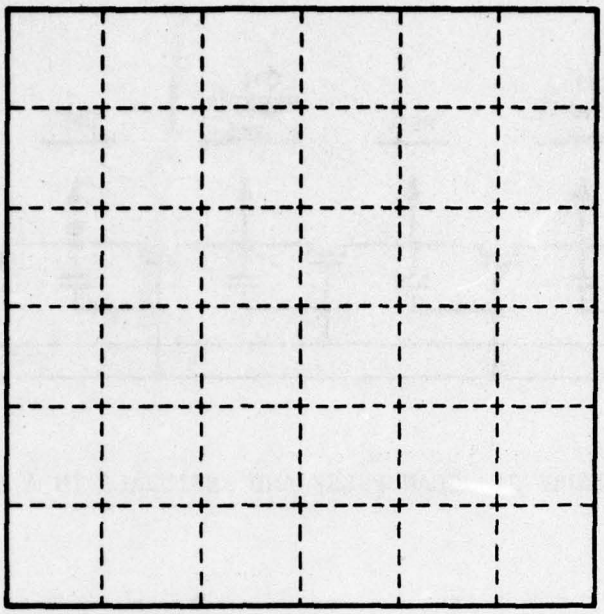

FIGURE 20 DES ... TO DESIRED EXTENT

2.3.5 Full TV Format Via DES Architecture

It is appropriate at this point to estimate the number of sectors (N_s) that would be used for a 512 x 512 TV format based solely on the BBD CTE thus far achieved. For simplicity it is assumed that the BBD is operating in the scan mode of Figure 3. For this case, only a single transfer is required between columns or rows, thus providing a one-to-one correspondence between the number of columns (and rows) and number of transfers required. Injecting a scan pulse into a BBD will result in a loss of amplitude with each transfer. This loss appears as a charge transfer inefficiency (CTI) residue strung out behind the transiting pulse, as indicated in Figure 21.

For a given number of required transfers, we must determine if the amplitude at the final transfer is sufficient to perform the function desired. In addition, the residuals at the other nodes must be sufficiently trivial to prevent false signals at those nodes. To do this, the final transfer amplitudes and residual levels are computed by means of Equation (1).

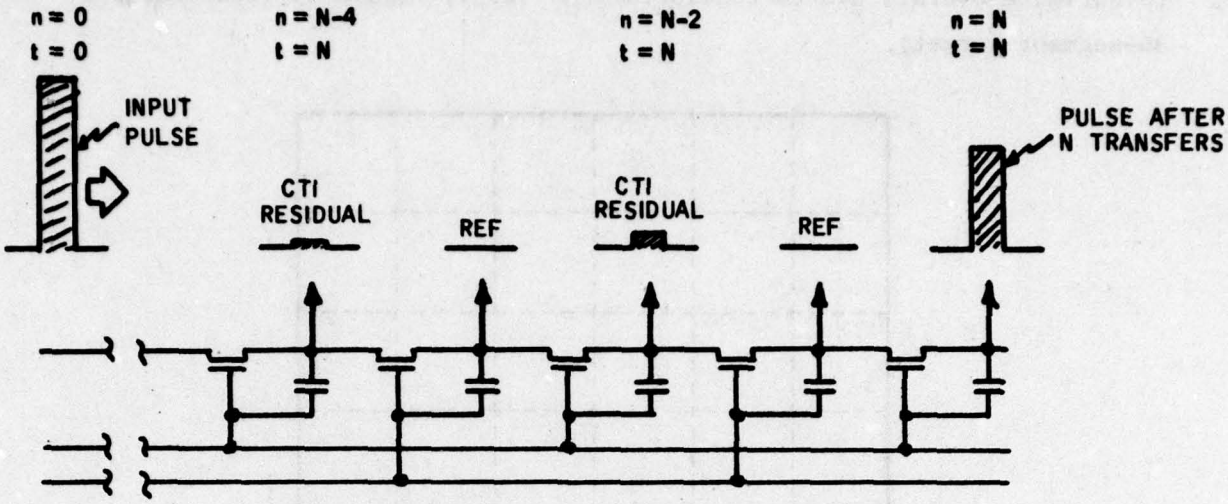

FIGURE 21 SCAN PULSE AND RESIDUALS IN A BBD

$$q(n,t) = \frac{\frac{t}{2}!}{\left(\frac{t}{2} - \frac{n}{2}\right)!\ \frac{n}{2}!}\ \alpha^{n}\ (2\varepsilon)^{\frac{t}{2} - \frac{n}{2}} \qquad (1)$$

The amplitude and residual leads are computed for each node using the time, t, and transfer number, n, indicated in Figure 21, where N represents the total number of transfers. It should be noted that although the pulse appears sequentially at every node, at any one moment in time, pulse and residuals will be separated by zero signal reference levels, as indicated in Figure 21. We thus calculate for every other node.

Taking trial values of N = 32, 64, and 128, the conditions obtained in Figure 22 can be illustrated. It should be noted that for the 32 and 64 transfer cases, the final amplitude and residuals are satisfactory for this mode of operation. However, the 128 transfer case is too marginal for consideration. A 32 x 32 sector would require 256 sectors, 64 x 64 64 sectors and 128 x 128 16 sectors. The 256-sector case is a bit difficult to work with, but the 64 sector case is reasonable. It is apparent that full TV format can be attained even with the relatively low values of CTE thus far

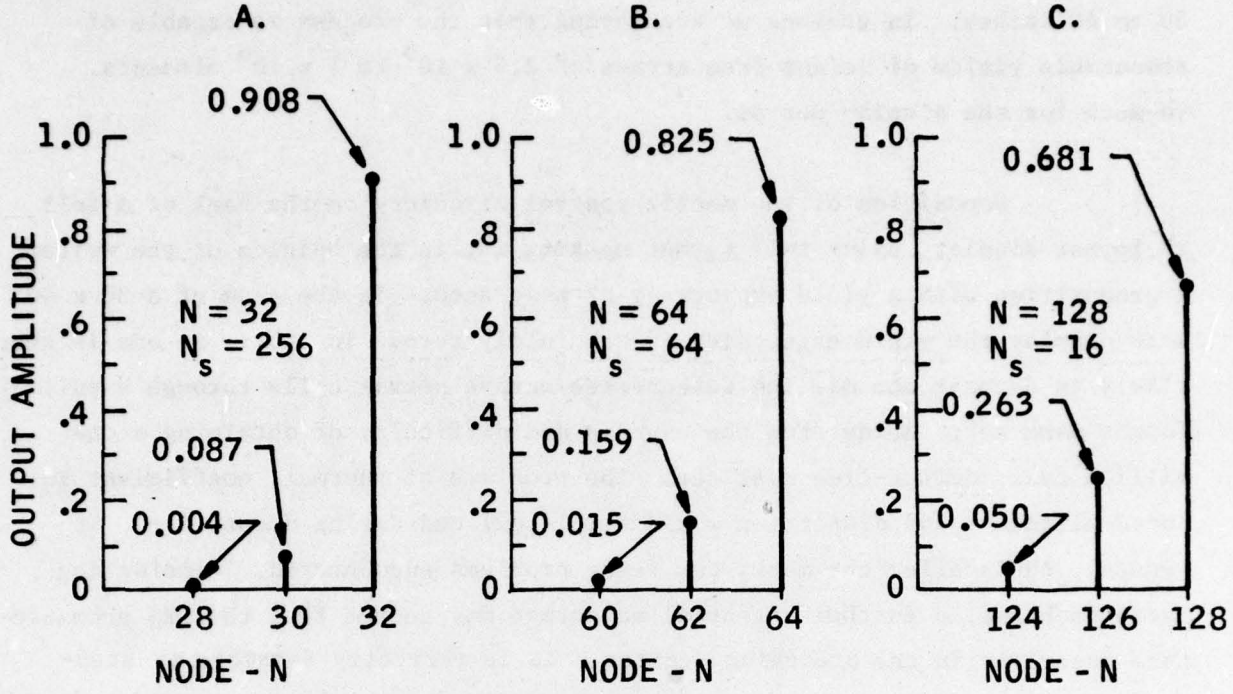

FIGURE 22 SPATIAL DISTRIBUTIONS AT FINAL TRANSFER VS TOTAL TRANSFERS, N, FOR CTE = 0.997 (ε = 0.003) WITH N_s REPRESENTING NUMBER OF SECTORS FOR 512 X 512 FORMAT

achieved. It should be noted, however, that increases in CTE are highly desirable since they would thus widen the choices in selection of the degree of DES required for overall system optimization and permit direct video transport modes of operation.

2.4 THE DES STEP-AND-REPEAT DISPLAY: A POSSIBLE APPROACH TO MATRIX CONTROL MASK VIABILITY

Thin film EL is an amazingly versatile display medium. It has no area limitations. Full, normal high resolution, single substrate TV formats can be produced from the limits of photolithography, on the small side, to dimensions of available glass plates and deposition facilities, on the large side. Single color, single substrate implementations require no in-chamber masking, up to the point of rear electrode formation, and none at all if this formation is done subtractively outside the deposition chamber. A reasonable yield of defect-free TV formats should be possible up to sizes of at least

30 to 40 inches. In essence, we are saying that the process is capable of reasonable yields of defect-free arrays of 2.5×10^5 to 1×10^6 elements. So much for the display per se.

Deposition of the matrix control circuitry on the back of a full TV format display, using full format masking is, in the opinion of the writer, a proposition with a yield expectancy of near zero. In the case of a 30 x 40 inch display, the yield expectancy is absolutely zero. In short, no one is ever likely to deposit one million defect-free active matrix cells through a full format mask set. Aside from the expense and difficulty of obtaining a one million cell defect-free mask set. The problems of thermal coefficient induced alignment and distortion would still be faced during deposition. In general, the smaller the mask, the fewer problems encountered. Considering these problems, a further potential advantage may accrue from the DES architecture described in the preceding section. It is perfectly feasible to step-and-repeat the matrix control pattern in the deposition chamber using small masks. The DES architecture suggests that these masks be designed to contain an integral number of DES sectors, since there are no connections between sectors and positioning precision would be relaxed. It is believed that the maximum mask size, for even very large displays (for example, over 30 x 40 inch case), should be limited to the order of 4 x 4 inches and down to perhaps 1 x 1 inch for small high-resolution displays.

The step-and-repeat concept may be a viable procedure for certain classes of displays. The procedure is, however, not likely to produce acceptable production line yields. The DES architecture can be implemented in other ways that promise greater producibility. These possibilities are examined in the following subsection.

2.5 THE DES MOSAIC DISPLAY: AN EXTREMELY VERSATILE HIGH-YIELD IMPLEMENTATION OF DES ARCHITECTURE

Historically, notions of physical modularization of flat-panel displays have been scoffed at because of the presumed requirement and difficulty of subsequently being forced to "re-connect" all the severed X and Y lines across

the entire display. DES architecture puts this objection to bed. There is no requirement to reconnect the X and Y lines, since within each sector these lines terminate in a BBD signal distribution circuit. It is only necessary to "pick up" a few lines from each sector. DES architecture offers the potential for building virtually any size display by forming a mosaic of fully self contained, independently operating small display modules. Each module has the matrix control circuitry deposited directly on the back of the display module per se. The concept is illustrated in Figure 23.

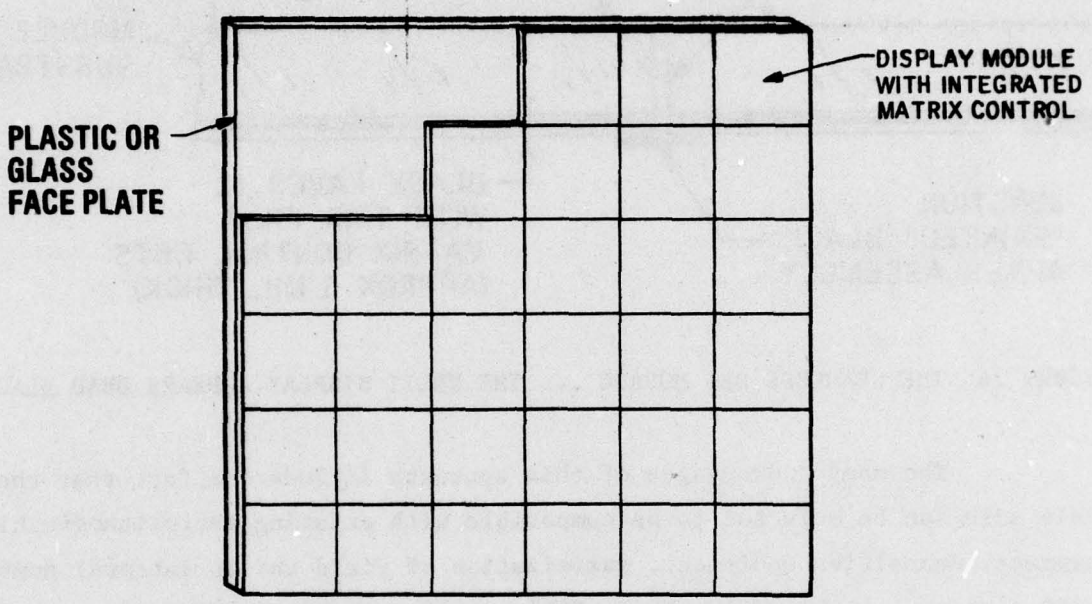

FIGURE 23 DES MOSAIC DISPLAY ... MADE PRACTICAL BY DES ARCHITECTURE

DES sector interconnect would again be as shown previously in Figure 19. Figure 23 implies that the modules are somehow bonded to a faceplate. The picture is intended only to illustrate the mosaic concept. In reality, the modules would most likely be placed face-up and optically aligned to form the mosaic, then vacuum cast in clear plastic to form the faceplate. Proper selection of the plastic index of refraction would prevent the module edges from being visible to the observer. Since our thin film EL contains a black layer, seemingly seamless mosaics can be completed by ensuring that the rear of all module junctions receive a black coating. These principles are illustrated in Figure 24.

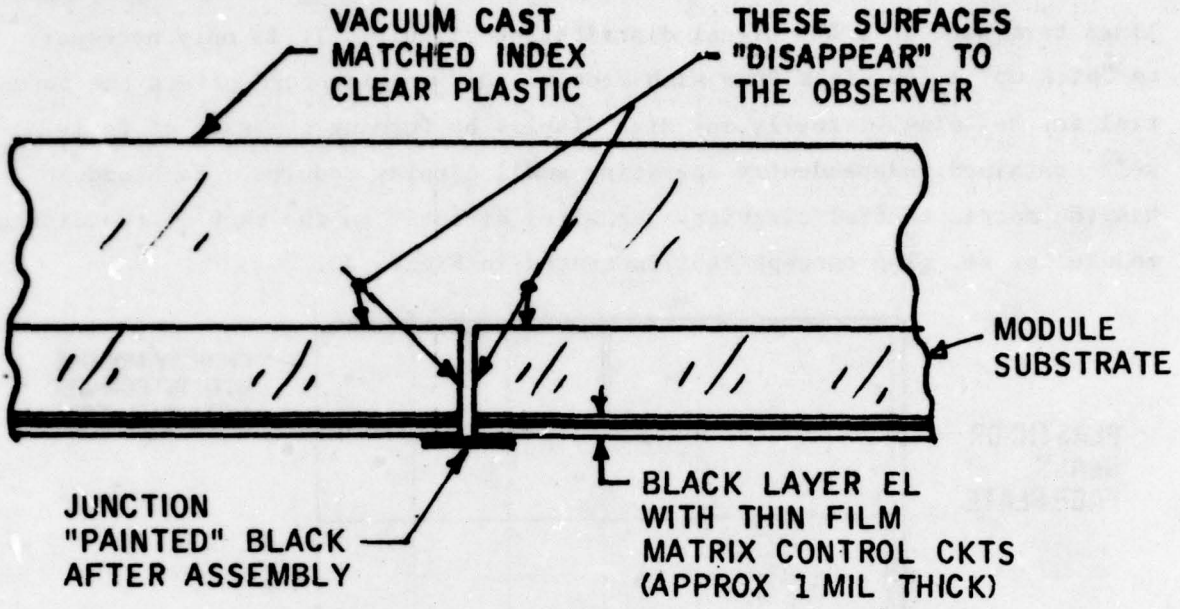

FIGURE 24 THE SEAMLESS DES MOSAIC ... THE UNLIT DISPLAY APPEARS DEAD BLACK

The many advantages of this approach include the fact that the module size can be selected to be compatible with existing photolithographic equipment, deposition equipment, maximization of yield and an integral number of DES sectors. Each module can be fully pretested and matched, if necessary, before assembly. Thus, although there will be a module production yield, complete displays can be expected to approach the 100-percent yield figure, since there is no functional interdependence between modules. In addition, one can envision, in principle, a module production system in which substrates go into the deposition chamber and display modules, complete with matrix control, come out ready for testing, having remained in a vacuum environment throughout the entire process.

There is absolutely no upper limit to the size of the finished display. Command and control dynamic displays can be conceived to be literally "wall" size. From a military application standpoint it is worth noting that penetration by a bullet or shell fragment would only incapacitate the particular module, or modules, involved. The remainder of the display would

continue to be operational. Given an appropriate repair "kit", such a display could be made field repairable.

It is believed that this approach to full TV format flat-panel displays is sufficiently versatile and producible to warrant the award of a program for its full development.

Section 3

CONCLUSIONS

It is concluded that full TV format display addressing can be accomplished with the modest bucket brigade device charge-transfer efficiency arrived at during this program. This has been made possible by a new matrix control architecture developed during the course of the program. In addition, the new architecture should make it physically possible to achieve the required high yield.

An unexpected factor which affects charge-transfer efficiency in a negative manner was uncovered. The subsequent solution resulted in a totally new, extremely versatile, active matrix that can be driven by low-voltage addressing circuitry including low-voltage thin film and MOS bucket brigade devices and other "IC" technology devices.

Section 4

RECOMMENDATIONS

The versatility of the matrix control compatible display modularization concept developed during this program should be applicable to a vast array of flat panel display requirements. It is recommended that a program be instituted to design, construct, assemble, and test a section of a flat-panel display to demonstrate the efficacy of the concept. It is also recommended that the program include further advances in charge-transfer efficiency of the bucket brigade devices which is so keyed to the concept.

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